Accurate capacitance and RC extraction software tool

for pixel, sensor, and precision analog designs

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This paper presents a new CAD tool – F3D – for accurate 3D capacitance and distributed RC model extraction for image sensor designs. Image sensor designs include many structures and circuits that are very sensitive to capacitive and resistive effects caused by metal interconnects and devices. These effects can be unintentional, i.e. parasitic – such as floating diffusion (FD) node capacitance being impacted by parasitic capacitance between metal/contact/poly structures, or delays along clock or signal nets caused by distributed RC effects, or intentional – such as capacitance of MIM or MOM structures used in sample and hold circuits, ADCs, and other circuits. F3D overcomes limitations of existing parasitic extraction tools and field solvers, and enables a predictive accurate capacitance extraction and distributed RC model generation, automated identification of all relevant capacitive coupling components, including long-range coupling, and detecting even small (down to 0.01% or better) capacitance mismatch caused by layout effects.

F3D is a rigorous field solver based on stochastic random walk method (see Figures 1 and 2), enabling capacitance extraction of complex three-dimensional large-area structures – such as pixels, arrays, and precision analog circuits (ADC, electrostatic shields, etc.). Unique features of the tool – user-definable capacitance calculation accuracy, mesh-less simulation method free from boundary condition and meshing artifacts, integration with standard physical verification flows, SPICE-compatible output (DSPF file), and ease of use – make it superior to existing popular parasitic extraction and field solver software tools. Application of F3D for calculation of floating diffusion (FD, or sense node) capacitance with varying metal layouts shows an excellent agreement with the measurement data. Examples of F3D application for other structures and circuits extraction are presented as well.

FD capacitance determines the pixel conversion gain, and it should be designed to a specific target value. Capacitance of small-size pixels is dominated by the coupling capacitances between the FD metal net and neighboring metals (Fig.3). Capacitance tuning can be easily achieved through metal layout optimization – provided that the capacitance extraction tool is reliable and accurate. Fig. 4 illustrates an excellent agreement between simulation and measurement results. F3D predicts the capacitance trend for varying metal layouts with absolute accuracy, and the total FD capacitance values with one-point calibration (F3D does not simulate semiconductor electrostatics and thus does not extract p-n junction and other non-linear capacitive semiconductor effects).

At the same time, F3D can be used as a general-purpose parasitic extraction tool providing guaranteed accuracy on large designs. One of breakthrough applications is super-high accuracy extraction of nets with nominally matched or weighted capacitances, such as in capacitor bank of SAR ADCs. Due to a close proximity of column ADCs (caused by pixel pitch constraint), parasitic coupling from the capacitor plates to the “outside world” violates prefect capacitance weighting and leads to integral and differential nonlinearities (INL and DNL) and loss of ADC resolution. F3D enables to detect capacitance mismatch as low as 0.01%, to identify the root causes of the mismatch, and thus to achieve a more reliable and higher performance designs from first silicon. It should be noted that MIM and MOM capacitors can be treated as interconnects and simulated with F3D, to achieve higher accuracy, rather than relying on simplistic device models utilized with most parasitic extraction tools (based on area and periphery capacitance components).

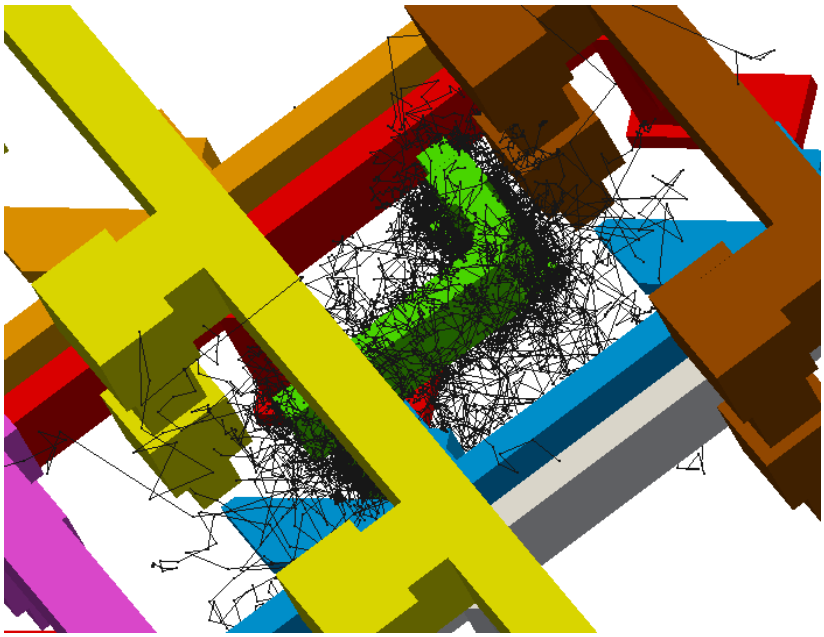

Fig.1. Illustration of the floating random walk method as applied for capacitance extraction problem. A large number of random walks (consisting of a series of hops) are started from the Gaussian surface of a net to get a statistical estimate of the capacitance coupling between this net and all other nets. Probabilities of hops are determined by Green's functions of the electrostatic potential. Random walks automatically find all the nets that are capacitively coupled to the net of interest.

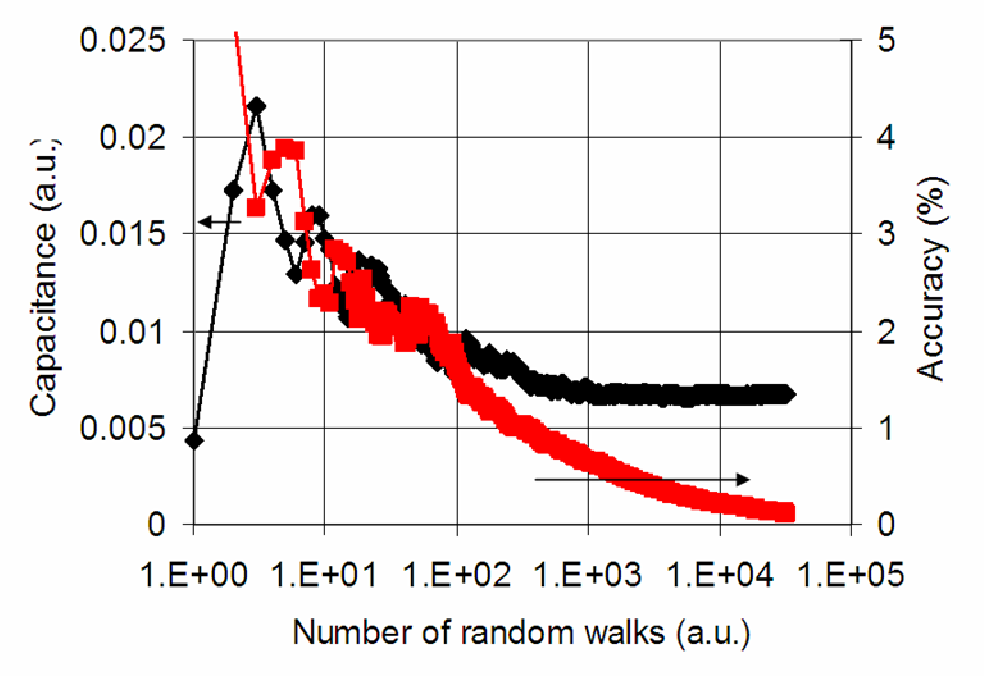

Fig.2. Illustration of random walk method convergence for calculated capacitance and reduction of statistical error of capacitance value with increase of the number of random walks.

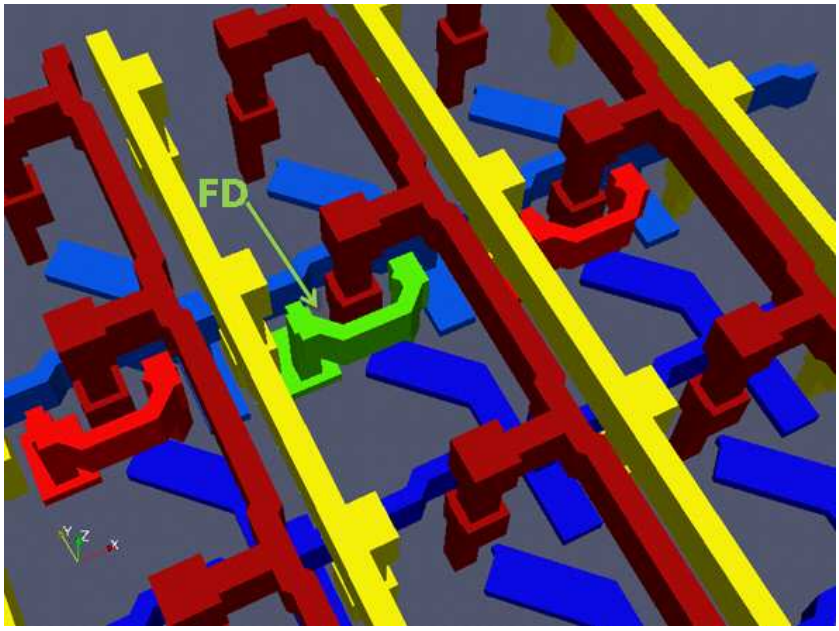

Fig.3. Example layout showing couplings between FD and neighboring metals.

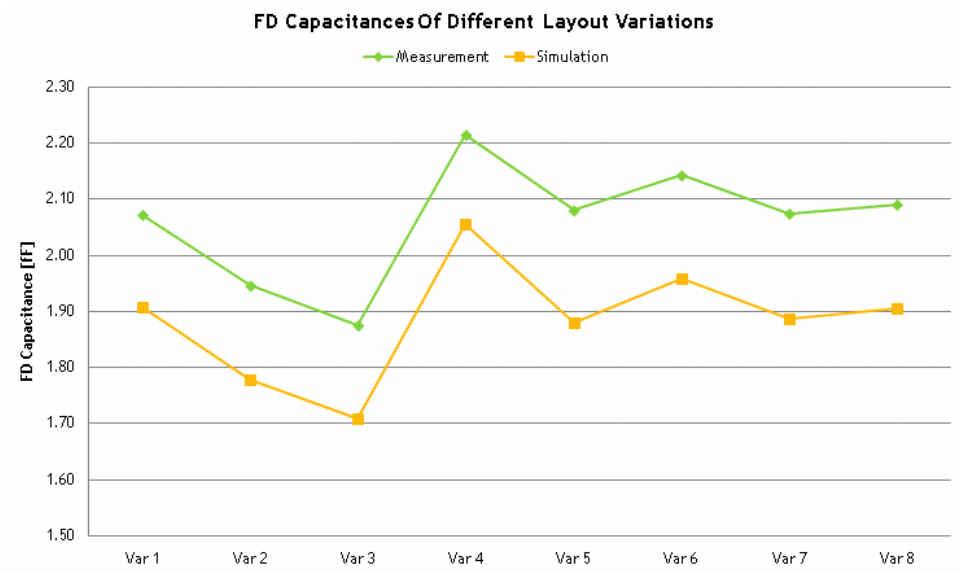

Fig.4. Comparison between measurement and simulation results of FD capacitance.